NINTENDO GAMECUBE™: The Ultimate Video Game Machine

Howard Cheng
Nintendo Technology Development
Technical Director

NINTENDO GAMECUBE

Nintendo®

The Vision

Nintendo: An Entertainment Company

"In first thinking about NINTENDO GAMECUBE five years ago, we envisioned a system which would allow us to create an environment which would surpass the common definition of video game play."

"To achieve this vision we built a system which is enabling an unprecedented rate of experimentation by the game development community. Experimentation can then lead to truly compelling new never before seen video games."

-- Mr. Genyo Takeda, General Manager of Integrated Research and Development, Nintendo Co., Ltd.

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Presenting…

NINTENDO GAMECUBE:

Launching in Japan on September 14, 2001
Launching in North America on November 5, 2001

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The Nintendo Difference

- Innovation
- In-house designers and engineers
- Game characters
- Heritage
- Focus - game creators in the driver's seat
- Quality

Success so far:

200 Million units of hardware sold

1.5 Billion units of software sold

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Hardware Partner Selection

- Technology Leadership
- Manufacturing Capability
- System Design and Innovation
- Intellectual Property
- Engineering Expertise and Experience

Console Design Goals

Simplicity of Design

- **Simplicity of architecture**
  - RISC architecture
  - PowerPC
- **Focus on game developer time to market**
  - Ease of creating software and games
  - Avoid HW induced development obstacles
- **Maximize achievable sustained performance**
  - Reduce system bottlenecks
  - Improve overall dataflow
- **Efficient board design**

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Console Hardware

- **IBM CPU – “Gekko”**
  - Game scripting, AI
  - Physics and collision detect
  - Custom effects & geometry
  - Custom and closeup lighting
- **ATI Graphics Processor – “Flipper”**
  - 3-D rendering, including lighting and geometry
- **MoSys memory – “Splash”**
  - 1T-SRAM – low latency
  - 24MB discrete and 3MB embedded

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Feedback So Far

Chris Stamper, President, Rare Ltd.:

"What really excites us about the machine is how easy it's going to be to work with. The new technology is really designed by people who understand games."

Dennis Dyack, President, Silicon Knights:

"While pushing more polygons is important, the true achievement lies in the perfection of the system. They have created the best video game performance rather than just the best polygon performance."

Right now, right here, great games…

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The Gekko Processor

Dean Amini

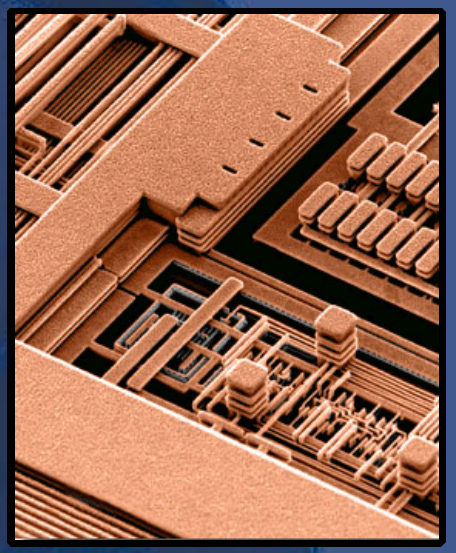
IBM® Microelectronics

Director, Advanced Personal Technologies

IBM technology

Why IBM?

- **Technology Leadership**
  - Enables leading edge products
  - Copper metallurgy and advanced interconnect & packaging
- **Manufacturing Capabilities**
  - High tech, mass market production
- **System Design and Innovation**
  - Leader in US patents for the last 7 years
  - Proven, stable design platforms
- **PowerPC® Architecture and IP**
  - Established, scalable from 50MHz to 1GHz
  - Easy to program



IBM technology

Gekko's Role

Programmers utilize Gekko to customize games

- **Game scripting, artificial intelligence (AI)**
- **Physics and collision detection**
  - Will Luigi run into walls? Through walls?
- **Custom effects, custom geometry**
- **Custom and close-up lighting**
  - Detail on Luigi's face

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Gekko Design Objectives

- **Leverage known games environment to maximize achievable, sustained system performance**
  - Implement custom gaming features on stable base
  - Utilize high performance PowerPC architecture and advanced technology
  - Minimize system bottlenecks
- **Focus on low cost mass manufacturing**
  - High reliability
  - Packaging
  - Efficient design

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Gekko Tradeoffs

- **Processor Organization**
  - *Options*: Single issue, superscalar, multi-core, multiprocessor
  - *Choice*: Superscalar for high performance, lower complexity
- **On-chip memory**
  - *Options*: L1 cache, L2 cache, embedded DRAM, SRAM
  - *Choice*: separate L1 caches, unified 256KB L2, L1 cache locking and DMA for efficient data movement
- **Floating point support**
  - *Options*: Single FP pipeline, dual pipeline, vector engine
  - *Choice*: Dual pipeline for higher performance while maintaining register architecture

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Easy to Program

- **PowerPC – well established, well known, RISC**
- **Developers writing games before NINTENDO GAMECUBE HW available**
  - Existing development kits, docs, support
  - Easy migration to final platform
- **Game Developers Kit (Nintendo)**
  - IDE with compiler, assembler, cross platform debugger
  - Nintendo optimization libraries to exploit Gekko features – character manipulation, math libraries, etc.

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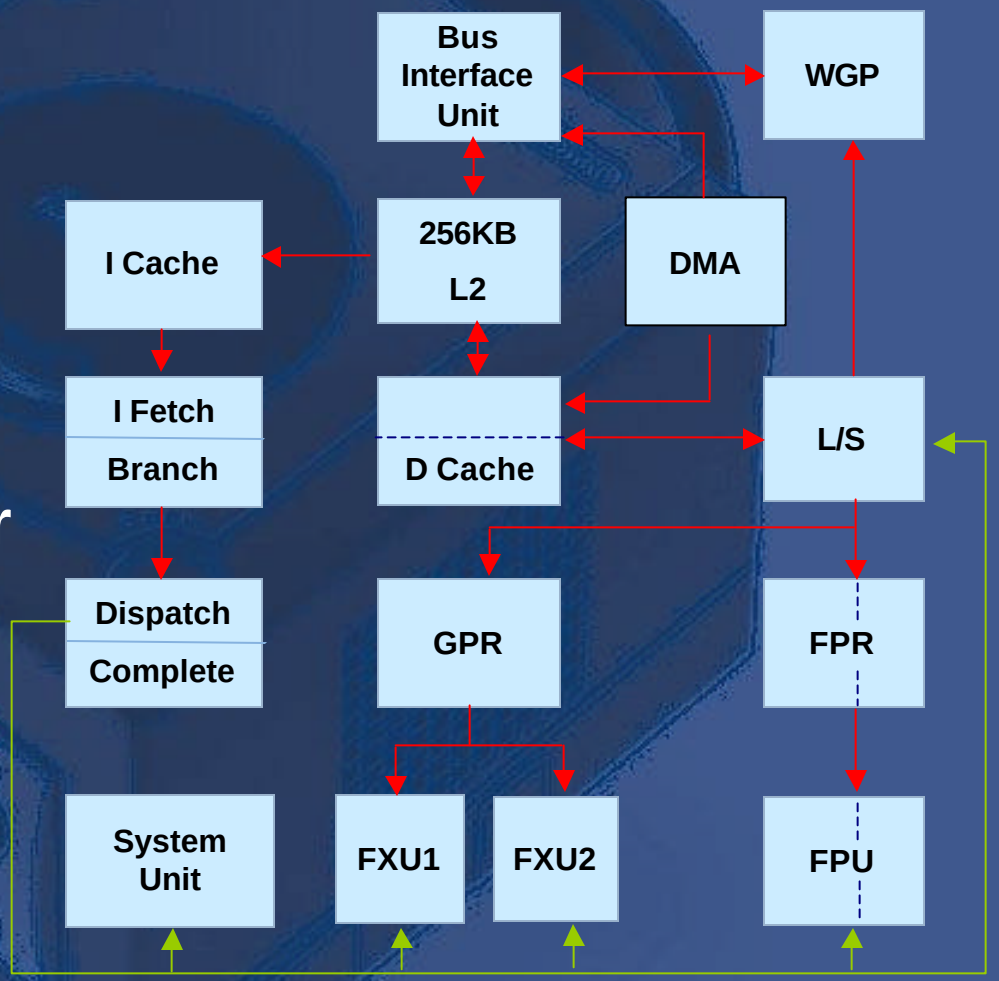
Gekko Block Diagram

- **PowerPC architecture with extensions that support:**
  - higher floating point throughput
  - higher bus bandwidth
- **38 new instructions for games optimizations**



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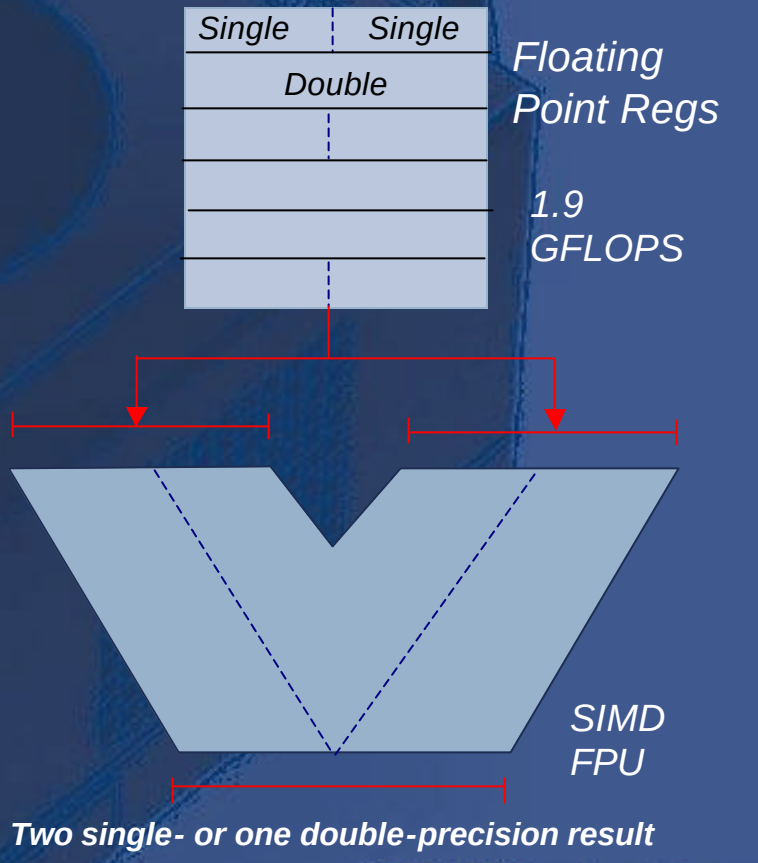
SIMD Floating Point

Acceleration for custom lighting and geometry calculations

- FPRs each hold one double-precision (DP) 64-bit operand or two single-precision (SP) 32-bit operands
- FPU performs one DP operation or two SP operations per cycle
- Pipelined multiply-add yields 4 fp ops per cycle for a peak throughput of 1.9 GFLOPS



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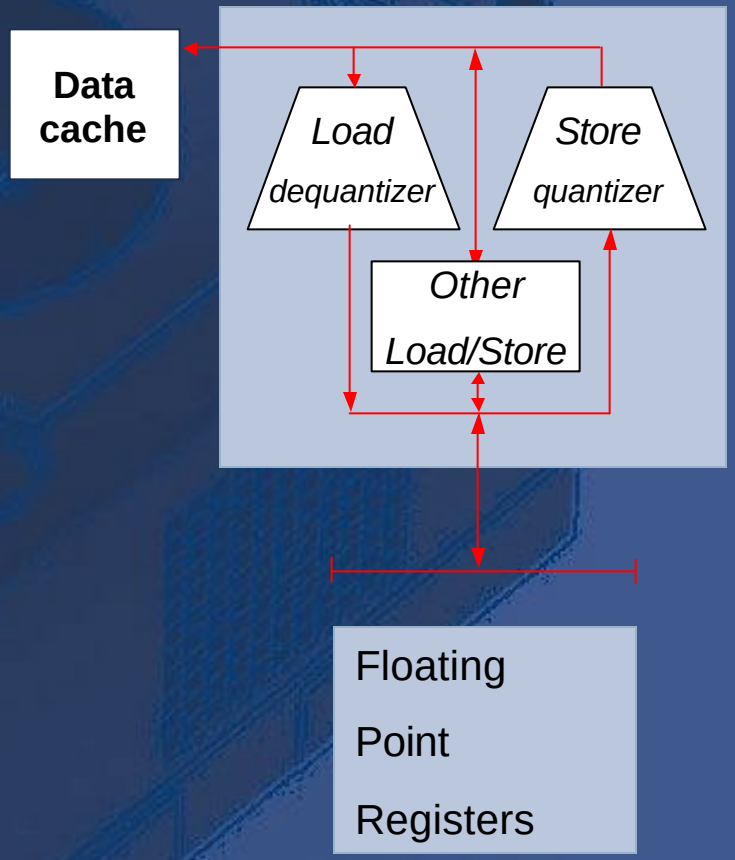
Data Compression

Can help reduce storage and bandwidth requirements

- **Load Q instruction:**
  - converts 8-bit or 16-bit integers to SP floating point
- **Store Q instruction:**
  - converts SP floating point to 8-bit or 16-bit integer
- **2:1 and 4:1 compression for graphics data**
  - Yields 5.2GB/s effective BW



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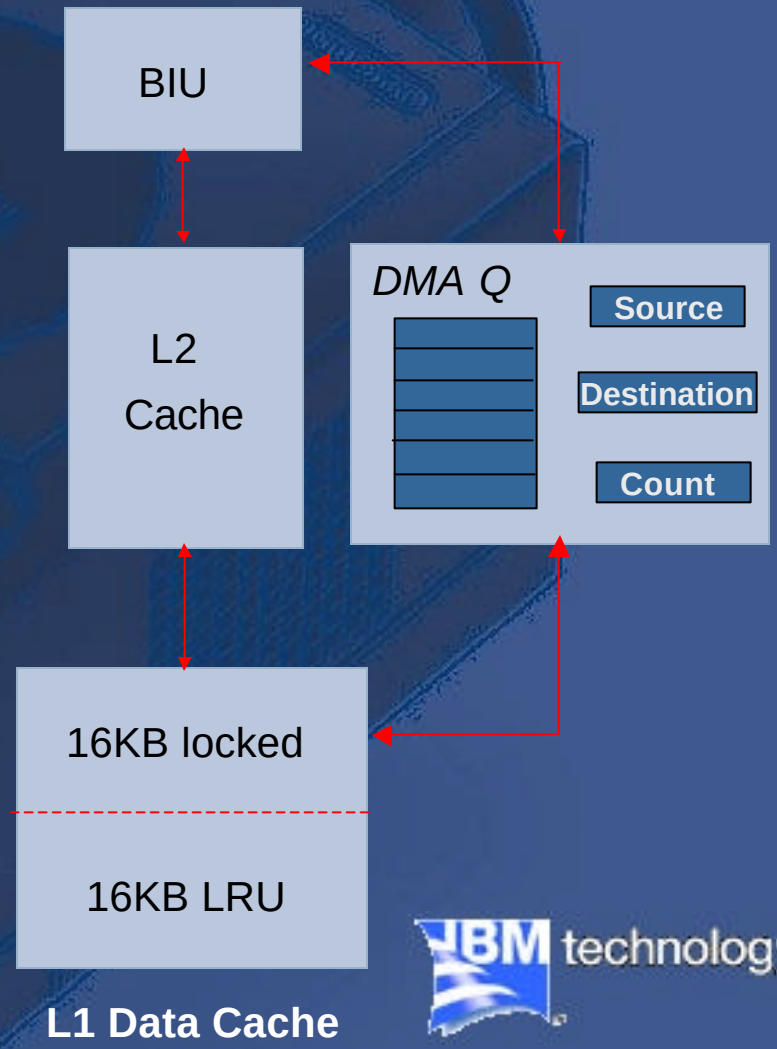
Cache Locking and DMA

L2 cache retains reusable but not transient data

- Data in locked half of D-cache can be transferred in parallel with instruction execution
- Transient data do not displace persistent data in L2 and unlocked L1
- Ideal for processing large, transient data sets such as object models, graphics commands, multimedia data



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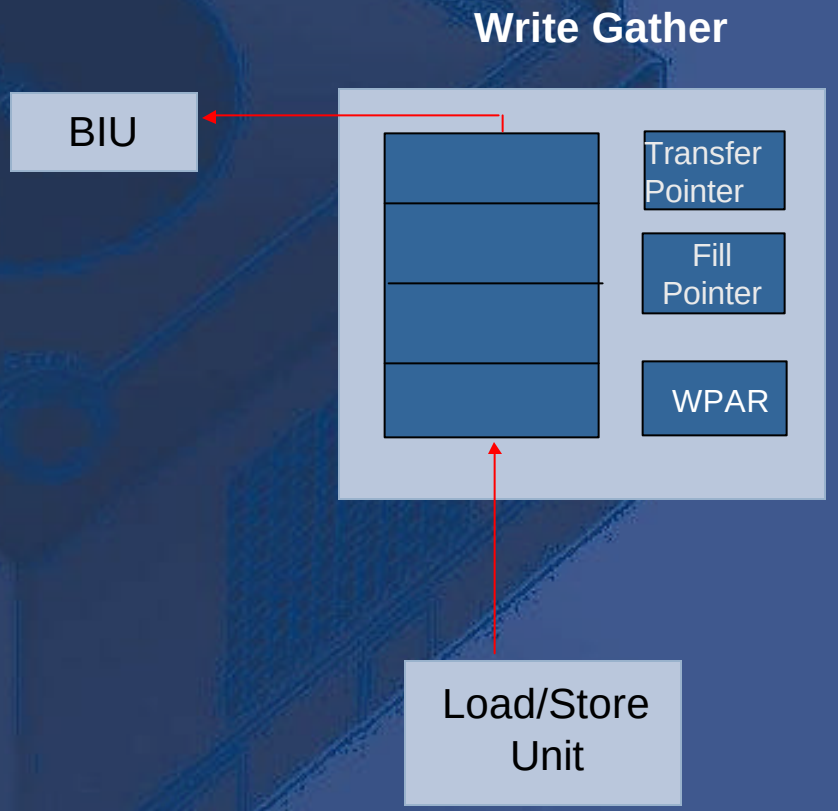
Write Gather Pipe

Efficient transfer of graphics commands and data to Flipper

- 128-byte FIFO gathers sequential non-cacheable stores to be transferred in parallel with instruction execution
- 32-byte block transfers over memory bus



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Gekko Specifications

Frequency - CPU	485MHz
Performance	1125 DMIPS (Dhrystone 2.1)
Power Dissipation	4.9W (typical)
Caches	L1: 32/32KB, 8-way set associative L2: 256KB, 2-way set associative
System Bus	1.3GB/s peak bandwidth (162MHz, 32-bit address, 64-bit data) 5.2GB/s effective with compression
Package	256 I/O, thermally enhanced 27x27mm PBGA
Technology	0.18µm CMOS copper technology, 6 levels of metal
Power Supply	1.8V logic and I/O

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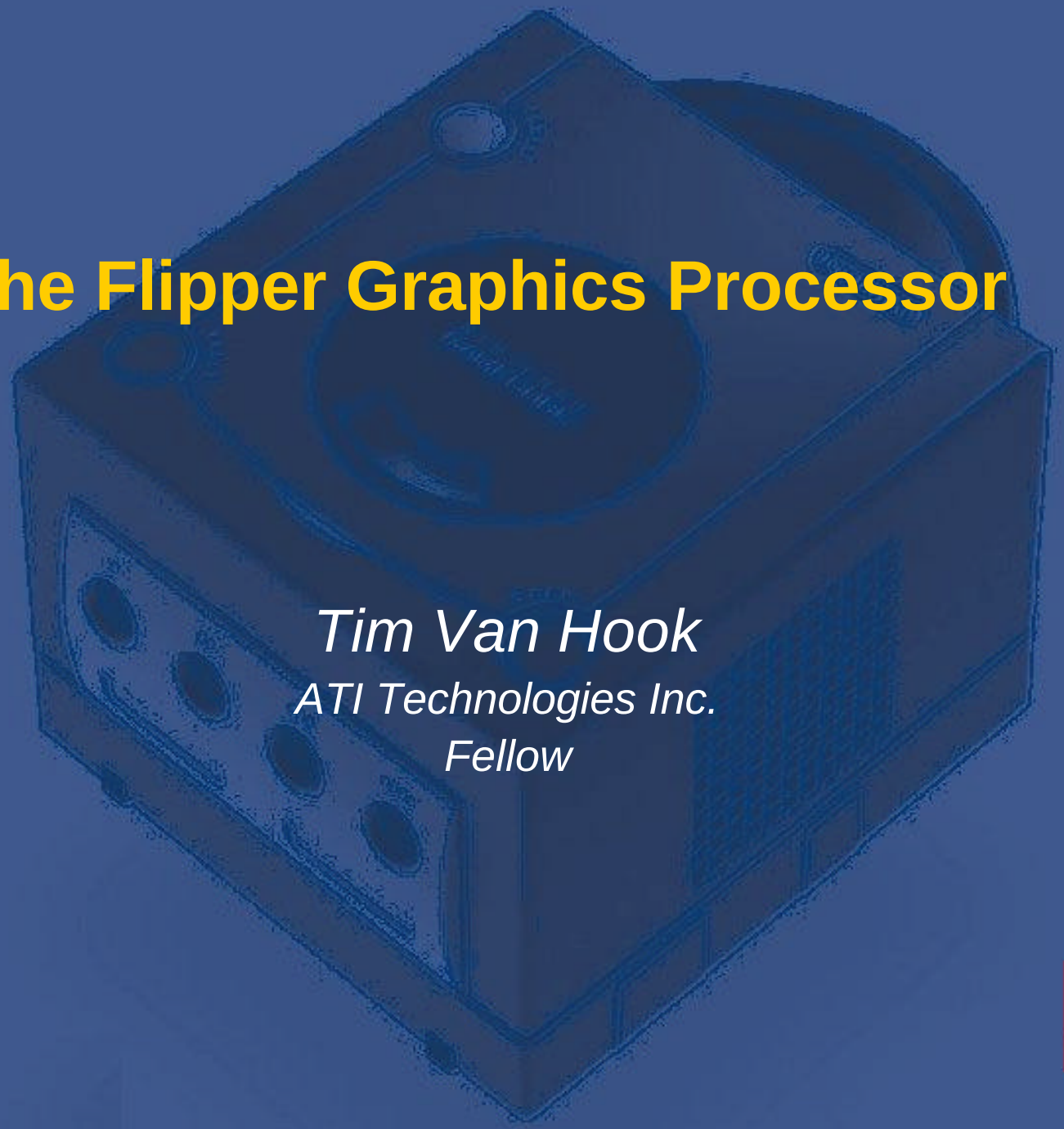
Summary

- **IBM chosen as design partner for proven leadership**
  - in technology, design, PowerPC architecture
- **IBM has delivered leadership**
  - in ease of development, to consumer market

Thank you!

IBM technology

The Flipper Graphics Processor



Tim Van Hook

ATI Technologies Inc.

Fellow

Memory

- **Audio Memory**
  - 16MB
  - 80MHz DRAM
- **“Splash” Main Memory**
  - 24MB
  - MoSys 1T-SRAM
  - 10ns sustainable latency

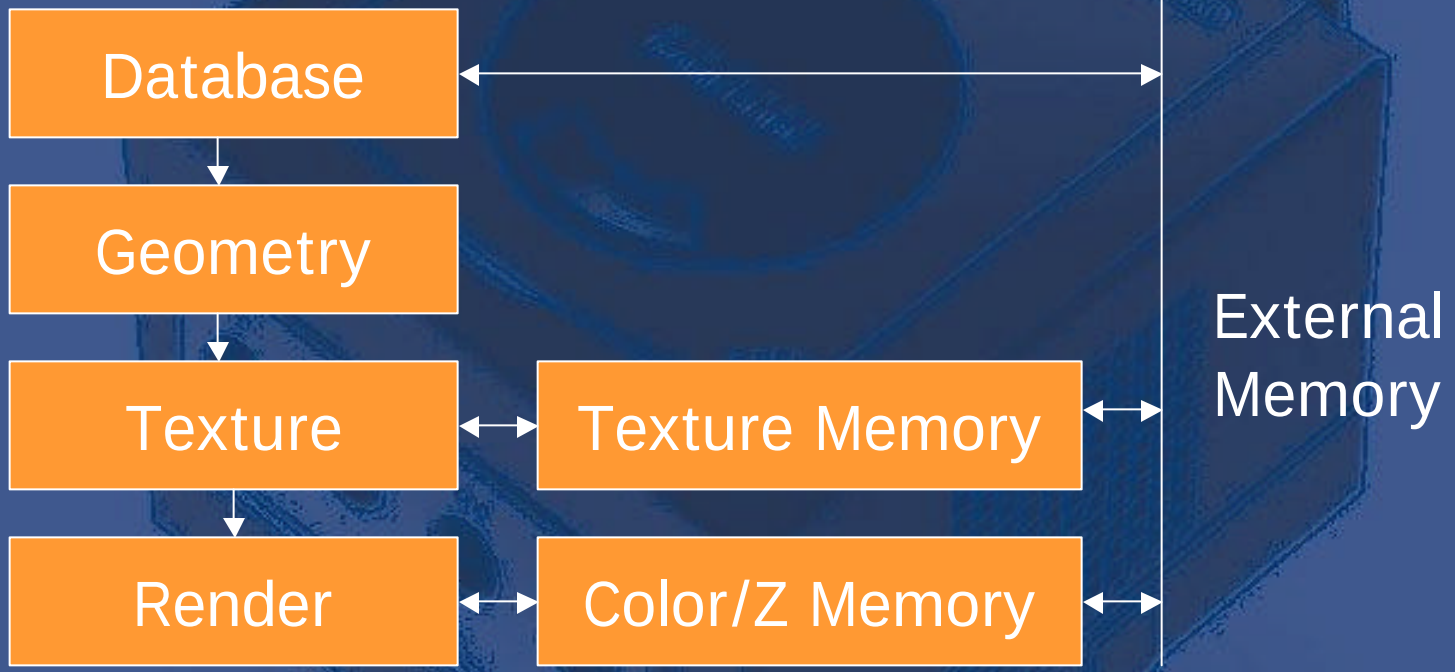
ATI Flipper System Chip

- Graphics Processor
- Audio Digital Signal Processor
- IO Processor
- 0.18㎜ NEC embedded DRAM process
- 500 pin BGA

Flipper Graphics Processor

- Full 3D hardware pipeline (database traversal, geometry and lighting, multi-texture and shading, color and Z rendering)
- Programmable lighting & shading modes
- Sub-pixel anti-aliasing and filtering
- Video processing
- Digital video interface to external DAC

Graphics Architecture



Flipper Audio DSP

- 16-bit DSP
- Instruction: 8KB RAM + 8KB ROM
- Data: 8KB RAM + 4KB ROM
- 64 channel ADPCM
- CD-quality 16-bit, 48KHz audio

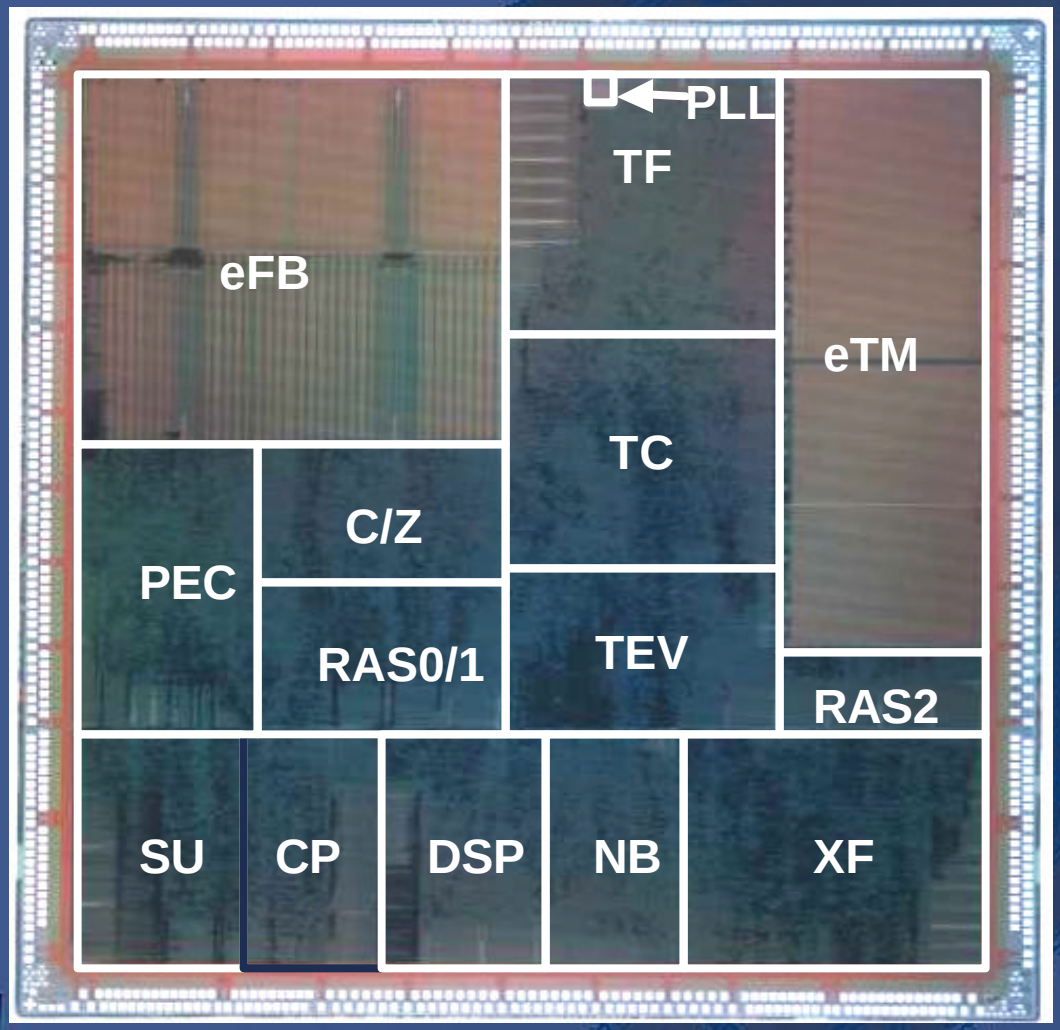
Flipper IO Processor

- Matsushita Optical Disc interface
- Game controller interface (x4)
- Digicard (memory card) interface (x2)
- High-speed serial port (x2)
- High-speed parallel port (x1)

Flipper Chip Statistics

- **51M transistors**
- **3.5M standard cell gates**
- **596Kb 2-port SRAM**
- **96Kb ROM**
- **24Mb MoSys 1T-SRAM**
  - 16Mb embedded Frame Buffer
  - 8Mb embedded Texture Cache

Flipper Die Photo



PLL = Phase Lock Loop
eFB = Embedded Frame Buffer
eTM = Embedded Texture Memory
TF = Texture Filter
TC = Texture Coordinate Generator
TEV = Texture Environment
RASx = Rasterizer
C/Z = Color/Z Calculator
PEC = Pixel Copy Engine
SU = Triangle Setup
CP = Command Processor
DSP = Audio DSP
XF = Triangle Transform Engine
NB = Northbridge - all system logic including CPU interface, Video Interface, Memory Controller, I/O Interface

Conclusion

- Achieved technology goals (schedule, performance, functionality, cost)
- But, it’s entertainment, not technology
- So, may the best games win

And now…

Star Wars Rogue Leader: Rogue Squadron II

Developer:
Factor 5, LLC

Publisher:
LucasArts Entertainment Company, LLC